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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/687,234	10/16/2003	Van Hoa Lee	AUS920030325US1	9433

35525 7590 03/23/2006

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EXAMINER	
RAHMAN, FAHMIDA	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 03/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/687,234	LEE, VAN HOA	
	Examiner	Art Unit	
	Fahmida Rahman	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/16/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-24 are pending.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 10/16/2003 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claim 24 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claim 24 recites a program product on a computer readable medium. However, it is not apparent that the computer readable medium is limited to tangible embodiment, since the medium can take the form of coded formats or, a transmission medium using light wave transmission, which may lack tangibility. For the rest of the office action, it is assumed that a tangible medium is intended.

Claim Objections

3. Claim 19 is objected to because of the following informalities:

"A-method" in line 1 should be changed to "A method".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 13, 16, 17 and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Zimmer et al (US Patent Application Publication 2004/0103272).

For claim 13, Zimmer et al teach the following limitations;

An apparatus comprising a processor (10), **a first memory** (20) **and a second memory** (16), **wherein the first memory comprises initialization code** (30 in Fig 3; [[0012] of page 1) **including a first portion** (first portion is executed from the ROM as shown in 30) **and a second portion** (second portion of the code is the code that is loaded in the cache), **the first portion having instructions for copying the first portion into the second memory** (the first portion must have some instruction to load the portion of code to the cache memory), **instructions for enabling instruction**

caching for the processor ([0013] of page 1), **and instructions for copying the second portion into a third memory** (40 of Fig 3 shows the copying to system memory. This must have associated instruction within the code for doing so).

For claim 16, first memory 20 is ROM.

For claim 17, second memory is cache 16 and 18 and third memory is the system memory 25.

For claim 18, execution steps are shown in Fig 3.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-8, 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zimmer et al (US Patent Application Publication 2004/0103272), in view of Nalawadi et al (US Patent No. 6704840).

For claim 1, Zimmer et al teach the following limitations:

A method of initializing an electronic device (Abstract), **comprising the steps of**:

- **beginning execution of initialization code** (30 in Fig 3; [[0012] of page 1) **in a first memory** (20) **to copy a first portion of the initialization code from the first memory** ([0013] of page 1 mentions that some of the early firmware code may be locked in 16. Thus, the portion of early firmware code is copied to cache memory) **into a second memory** (16);

- **continuing execution of the initialization code in the first memory** (30 in Fig 3; [[0012] of page 1) **to instruction caching** (The system continues execution of initialization code from ROM as shown in 30, until the code is locked in cache, as shown in 32. The instruction cache should be enabled to initiate locking as mentioned in [0013] of page 1. Thus, the initialization code is executed from first memory and instruction caching is performed as the code is loaded to I-Cache for further execution);
- **and executing at least some of the first portion of initialization code copied into the second memory** ([0019] of page 2).

Zimmer et al do not explicitly mention that the I-Caching is software enabled, although, Zimmer et al mention that the cache locking is software enabled ([0014] of page 1) and the I-Cache may be enabled to initiate locking for dedicated use in initialization. The initialization is controlled by pre-boot software and it is likely that the cache is enabled by software, since the cache enabling is done in pre-boot time.

Nalawadi et al teach a system where cache is enabled by software control ([0053] of page 4).

It would have been obvious to one ordinary skill in the art at the time the invention was made to combine the teachings of Zimmer et al and Nalawadi et al. One ordinary skill in the art would have been motivated to have a cache with software control in the system of Zimmer et al, since the system is yet to be initialized. During initialization, cache settings are changed repeatedly as shown in 32, 34, 36, 40 of Zimmer et al. Thus, the cache enabling done by pre-boot software, as mentioned explicitly in Nalawadi et al, would favor the speed of the system ([0023] of Nalawadi et al).

For claims 2 and 3, [0015] of page 1 of Zimmer et al mention that the data cache stores some initialization data that is copied to system memory as shown in 40 of Fig 3. The initialization code has to be executed in system memory to finish the initialization. Thus, the second portion of initialization code is copied to third memory and executed from system memory.

For claim 4, the cache is disabled at the beginning since the process starts at 28 in Zimmer et al, which is the power on reset. Cache is enabled later to lock the code in cache. Thus, cache must be disabled at the beginning.

For claim 5, instruction caching is enabled during execution of some of initialization code as mentioned in [0012] and [0013] of page 1 in Zimmer et al.

For claim 6, the system does not disable the instruction caching in 36-42 in Fig 3 of Zimmer et al. Thus, I-cache is enabled during the execution of second portion.

For claim 7, first memory 20 of Zimmer et al is ROM.

For claim 8, second memory is cache 16 and 18 and third memory is the system memory 25 (Zimmer et al).

For claim 19, Zimmer et al teach the following limitations;

A method for initializing an apparatus comprising a first memory (20) **and second memory** (16 and 18), **the first memory having apparatus initialization code stored therein** ([0011]), **comprising the steps of:**

- **executing at least some of the initialization code in the first memory to copy a first portion of the initialization code from the first memory to the second memory** (30, 32, 34, 36 in Fig 3);

- **executing at least some of the initialization code in the first memory to enable instruction caching** (The system continues execution of initialization

code from ROM as shown in 30, until the code is locked in cache, as shown in 32. The instruction cache is enabled to initiate locking as mentioned in [0013] of page 1. Thus, the initialization code is executed from first memory and instruction caching is performed as the code is loaded to I-Cache for further execution);

- **and executing at least some of the first portion of the initialization code in the second memory** ([0019] of page 2) **to copy a second portion of initialization code from the first memory to a third memory** ([0015] of page 1 mention that the data cache stores some initialization data that is copied to system memory as shown in 40. The initialization code has to be executed in system memory to finish the initialization. The code that is executed from the system memory to finish initialization can be considered second portion of the code).

Zimmer et al do not explicitly mention that the I-Caching is software enabled, although, Zimmer et al mention that the cache locking is software enabled ([0014] of page 1) and the I-Cache may be enabled to initiate locking for dedicated use in initialization. The initialization is controlled by pre-boot software and it is likely that the cache is enabled by software, since the cache enabling is done in pre-boot time.

Nalawadi et al teach a system where cache is enabled by software control ([0053] of page 4).

It would have been obvious to one ordinary skill in the art at the time the invention was made to combine the teachings of Zimmer et al and Nalawadi et al. One ordinary skill in the art would have been motivated to have a cache with software control in the system of Zimmer et al, since the system is yet to be initialized. During initialization, cache settings are changed repeatedly as shown in 32, 34, 36, 40 of Zimmer et al. Thus, the cache enabling done by pre-boot software, as mentioned explicitly in Nalawadi et al, would favor the speed of the system ([0023] of Nalawadi et al).

For claim 20, note 42 of Zimmer et al.

For claim 21, cache is enabled by the system when code is loaded to cache. Thus, cache is disabled before enabling the cache.

For claim 22, note 32 of Zimmer et al.

For claim 23, I-Cache is continued to be enabled once it is first enabled.

6. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zimmer et al (US Patent Application Publication 2004/0103272), in view of Nalawadi et al (US Patent No. 6704840), further in view of Dawson (US Patent Application Publication 2004/0025145).

For claim 9, the system of Zimmer et al, as modified by Nalawadi et al, does not mention that the cache enabling code is located at the end of the page.

Dawson teaches a system where cache enabling routine is located at the end of the page (94 of Fig 2).

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Zimmer et al, Nalawadi et al and Dawson. One ordinary skill in the art would have been motivated to have cache enabling routine at the end of the page as disclosed in Dawson, in the system of Zimmer et al as modified byNalawadi et al, since that would be useful for execution of specific code outside the cache memory as shown in Dawson.

For claim 10, the page is not initialized until the cache is enabled and load the page to cache.

7. Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Avraham (US Patent Application Publication 2003/0233533), in view of Springer et al (US Patent 6212631), further in view of Dawson (US patent Application Publication 20040025145).

For claim 11, Avraham teaches the following limitations:

An apparatus, comprising:

a first memory organized as a plurality of memory pages, wherein the first memory has initialization code stored therein (lines 8-14 of [0009] mention that NAND flash memory is storing the boot code).

Avraham does not teach the following limitations:

the initialization code having an instruction cache enabling routine located at an end of one of the memory pages.

Springer et al teach the following limitations:

BIOS code including cache enabling routine (abstract mentions that BIOS includes cache support feature, which in turn includes code for enabling cache ECC)

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Avraham and Springer et al. One ordinary skill in the art would have motivated to set cache enabling routine within the initialization routine, since it would provide the user a choice to enable cache during initialization, since cache is well known for its faster speed.

However, the combination of Avraham and Springer et al does not teach that the cache enabling routine is located at the end of the page.

Dawson teaches a system where cache enabling routine is located at the end of the page (94 of Fig 2).

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Avraham, Springer et al and Dawson. One ordinary skill in the art would have been motivated to have cache enabling routine at the end of the page as disclosed in Dawson, in the system of Avraham as modified by Springer et al, since that would be useful for execution of specific code outside the cache memory as shown in Dawson.

For claim 12, the page is not initialized until it is executed.

8. Claims 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zimmer et al (US Patent Application Publication 2004/0103272), in view of Avraham (US Patent Application Publication 2003/0233533), further in view of Springer et al (US Patent 6212631), further in view of Dawson (US patent Application Publication 20040025145).

For claim 14, Zimmer et al do not teach that the memory is organized as a plurality of memory pages and cache enabling code is located at a memory page boundary.

Avraham teaches the following limitations:

An apparatus, comprising:

a first memory organized as a plurality of memory pages, wherein the first memory has initialization code stored therein (lines 8-14 of [0009] mention that NAND flash memory is storing the boot code).

Avraham does not teach the following limitations:

the initialization code having an instruction cache enabling routine located at an end of one of the memory pages.

Springer et al teach the following limitations:

BIOS code including cache enabling routine (abstract mentions that BIOS includes cache support feature, which in turn includes code for enabling cache ECC)

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Avraham and Springer et al. One ordinary skill in the art would have motivated to set cache enabling routine within the initialization routine, since it would provide the user a choice to enable cache during initialization, since cache is well known for its faster speed.

However, the combination of Avraham and Springer et al does not teach that the cache enabling routine is located at the end of the page.

Dawson teaches a system where cache enabling routine is located at the end of the page (94 of Fig 2).

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Avraham, Springer et al and Dawson. One ordinary skill in the art would have been motivated to have cache enabling routine at the end of the page as disclosed in Dawson, in the system of Avraham as modified by Springer et al, since that would be useful for execution of specific code outside the cache memory as shown in Dawson.

For claim 15, the page is not initialized until the cache is enabled and load the page to cache.

Claim 24 is directed to the storage required to implement the method of claim 1. As storage is required to store the instructions that implements a method, the cited reference that teach the invention for claim 1 also teaches the invention disclosed by claim 24.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fahmida Rahman whose telephone number is 571-272-8159. The examiner can normally be reached on Monday through Friday 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on 571-272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Fahmida Rahman
Examiner
Art Unit 2116

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